WHAT IS CLAIMED IS:

1. A random access memory (RAM) comprising:

an array of memory cells arrange in a plurality of rows and columns wherein access of each row is based on a wordline signal; and

a wordline circuit receiving a positive voltage at a voltage node, receiving a decoding signal representative of an idle mode at a decoding node, and providing to at least one of the rows of memory cells a wordline signal based on the decoding signal and forming a leakage path from the voltage node to a reference node when the decoding signal indicates the idle mode.

2. The memory of claim 1, wherein the memory cells comprises DRAM memory cells.

3. The memory of claim 1, wherein the reference node is a ground reference.

4. The memory of claim 1, wherein the wordline circuit further comprises:

a latch configured to hold a state of the decoding node;

a translation block configured to provide a voltage level at a bar decode node based on the decoding signal; and

an output block configured to provide the wordline signal at an output node based on the voltage level.

5. The memory of claim 4, wherein the latch comprises a PMOS transistor having a gate coupled to the bar decode node, a source coupled to the voltage node, and a drain coupled to the decode node.

6. The memory of claim 4, wherein the translation block further comprises:

a PMOS transistor having a gate coupled to the decode node, a source coupled to the voltage node, and a drain coupled to the bar decode node; and

an NMOS transistor having a gate coupled to the decode node, a drain coupled to the bar decode node, and a source coupled to the reference node.

7. The memory of claim 6, wherein the leakage path comprises a path from the voltage node to the reference node via the PMOS transistor and the NMOS transistor of the translation block.

8. The memory of claim 4, wherein the output block further comprises:

a first PMOS transistor having a gate coupled to the bar decode node, a source coupled to the voltage node, and a drain coupled to the output node;

a second PMOS transistor having a gate coupled to the reference node, a source coupled to the bar decode node, and a drain;

a first NMOS transistor having a gate coupled to the output node, a drain coupled to the drain of the second PMOS transistor, and a source coupled to a negative voltage node receiving a negative voltage from an external power source; and

a second NMOS transistor having a gate coupled to the drain of the second PMOS transistor, a drain coupled to the output node, and a source coupled to the negative voltage node.

9. A wordline circuit use in a random access memory (RAM), the wordline circuit receiving a positive voltage at a voltage node, receiving a decoding signal representative of a self-refresh mode at a decoding node, and providing a wordline signal based on the decoding node and forming a current leakage path from the voltage node to a reference node when the decoding signal indicates the self-refresh mode.

10. The wordline circuit of claim 9, wherein the reference node comprises a ground node.

11. The wordline circuit of claim 9 further comprising:

a latch configured to hold a state of the decoding node;

a translation block configured to provide a voltage level at a bar decode node based on the decoding signal; and

an output block configured to provide the wordline signal at an output node based on the voltage level.

12. The wordline circuit of claim 11, wherein the latch comprises a PMOS transistor having a gate coupled to the bar decode node, a source coupled to the voltage node, and a drain coupled to the decode node.

13. The wordline circuit of claim 11, wherein the translation block further comprises:

a PMOS transistor having a gate coupled to the decode node, a source coupled to the voltage node, and a drain coupled to the bar decode node; and

an NMOS transistor having a gate coupled to the decode node, a drain coupled to the bar decode node, and a source coupled to the reference node.

14. The wordline circuit of claim 13, wherein the leakage path comprises a path from the voltage node to the reference node via the PMOS transistor and the NMOS transistor of the translation block.

15. The wordline circuit of claim 11, wherein the output block further comprises:

a first PMOS transistor having a gate coupled to the bar decode node, a source coupled to the voltage node, and a drain coupled to the output node;

a second PMOS transistor having a gate coupled to the reference node, a source coupled to the bar decode node, and a drain;

a first NMOS transistor having a gate coupled to the output node, a drain coupled to the drain of the second PMOS transistor, and a source coupled to a negative voltage node receiving a negative voltage from an external power source; and

a second NMOS transistor having a gate coupled to the drain of the second PMOS transistor, a drain coupled to the output node, and a source coupled to the negative voltage node.

16. A row decoder for use in a random access memory (RAM), comprising:

a decoder unit decoding an externally inputted precharge signal and externally inputted row address signals, and providing a decoding signal representative of an idle state; and

a wordline circuit receiving a positive voltage at a voltage node, receiving the decoding signal at a decode node, providing a wordline signal based on the decoding signal, and forming a current leakage path from the voltage node to a reference node when the decoding signal indicates the idle state.

17. The row decoder of claim 16, wherein the decoder unit further comprises:

a PMOS transistor receiving the precharge signal at a gate, having a source coupled to the voltage node, and a drain coupled to the decode node;

a first NMOS transistor receiving a first address signal at a gate, having a drain coupled to the decode node, and a source;

a second NMOS transistor receiving a second address signal at a gate, having a drain coupled to the source of the first NMOS transistor, and a source; and

a third NMOS transistor receiving a third address signal at a gate, having a drain coupled to the source of the second NMOS transistor, and a source coupled to a reference node.

18. The row decoder of claim 16, wherein the reference node is ground.

19. The row decoder of claim 16, wherein the driver circuit further comprises:

a latch configured to hold a state of the decoding node;

a translation block configured to provide a voltage level at a bar decode node based on the decoding signal; and

an output block configured to provide the wordline driver signal at an output node based on the voltage level.

20. The row decoder of claim 19, wherein the latch comprises a PMOS transistor having a gate coupled to the bar decode node, a source coupled to the voltage node, and a drain coupled to the decode node.

21. The row decoder of claim 19, wherein the translation block further comprises:

a PMOS transistor having a gate coupled to the decode node, a source coupled to the voltage node, and a drain coupled to the bar decode node; and

an NMOS transistor having a gate coupled to the decode node, a drain coupled to the bar decode node, and a source coupled to the reference node.

22. The row decoder of claim 21, wherein the leakage path comprises a path from the voltage node to the reference node via the PMOS transistor and the NMOS transistor of the translation block.

23. The row decoder of claim 19, wherein the output block further comprises:

a first PMOS transistor having a gate coupled to the bar decode node, a source coupled to the voltage node, and a drain coupled to the output node;

a second PMOS transistor having a gate coupled to the reference node, a source coupled to the bar decode node, and a drain;

a first NMOS transistor having a gate coupled to the output node, a drain coupled to the drain of the second PMOS transistor, and a source coupled to a negative voltage node receiving a negative voltage from an external power source; and

a second NMOS transistor having a gate coupled to the drain of the second PMOS transistor, a drain coupled to the output node, and a source coupled to the negative voltage node.

24. A method of reducing leakage current of a driver circuit during an idle mode of a random access memory, the method comprising:

receiving a decoding signal representative the idle mode;

receiving a positive voltage from an external power source at a voltage node; and

forming a leakage path from the voltage node to a reference node when the decoding signal indicates the idle mode.

25. The method of claim 24, wherein the reference node is ground.

26. A method of reducing losses in a random access memory (RAM) having a driver circuit receiving a positive voltage from a voltage source, the method comprising:

receiving a decoding signal having a state representative of an idle mode; and

forming a current leakage path from the voltage source to a reference node when the state of the decoding signal represents the idle mode.

27. The method of claim 26, wherein the reference node is ground.